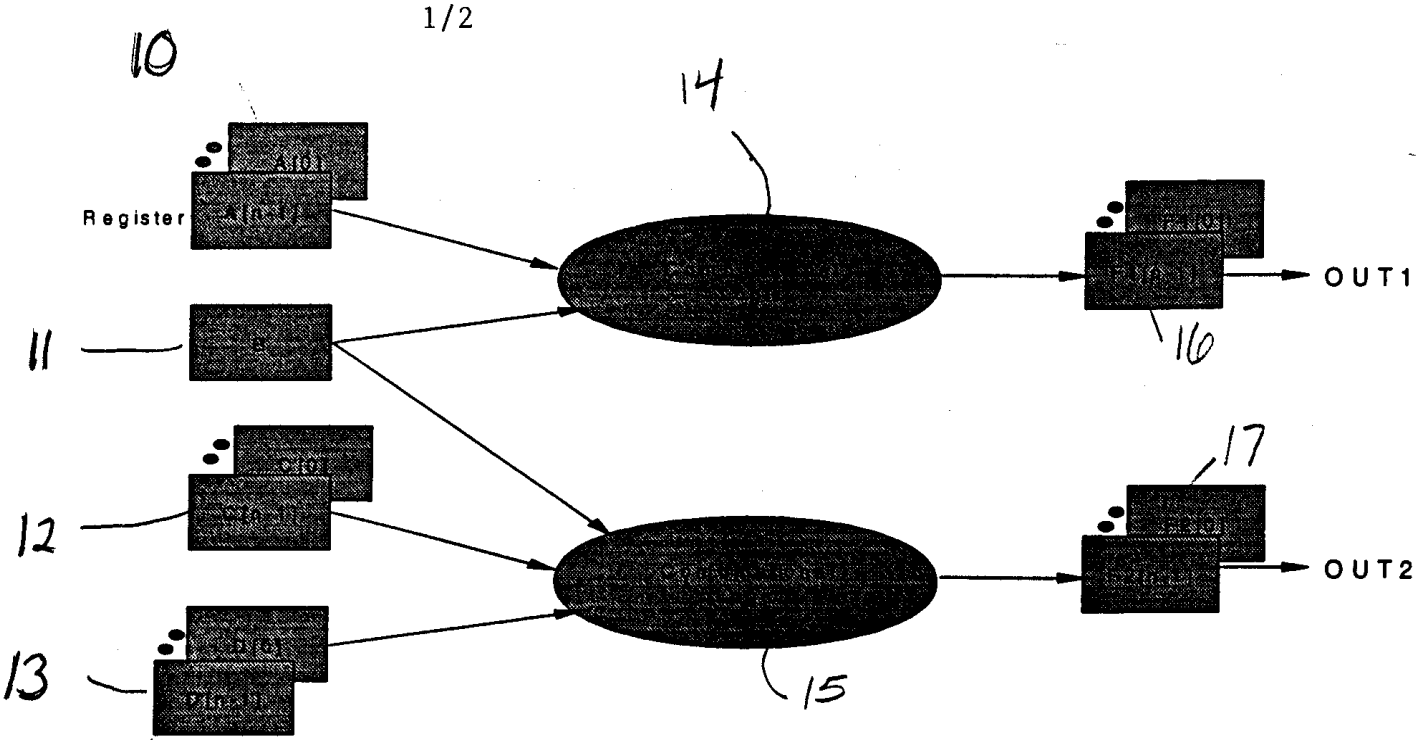

Figure 1A

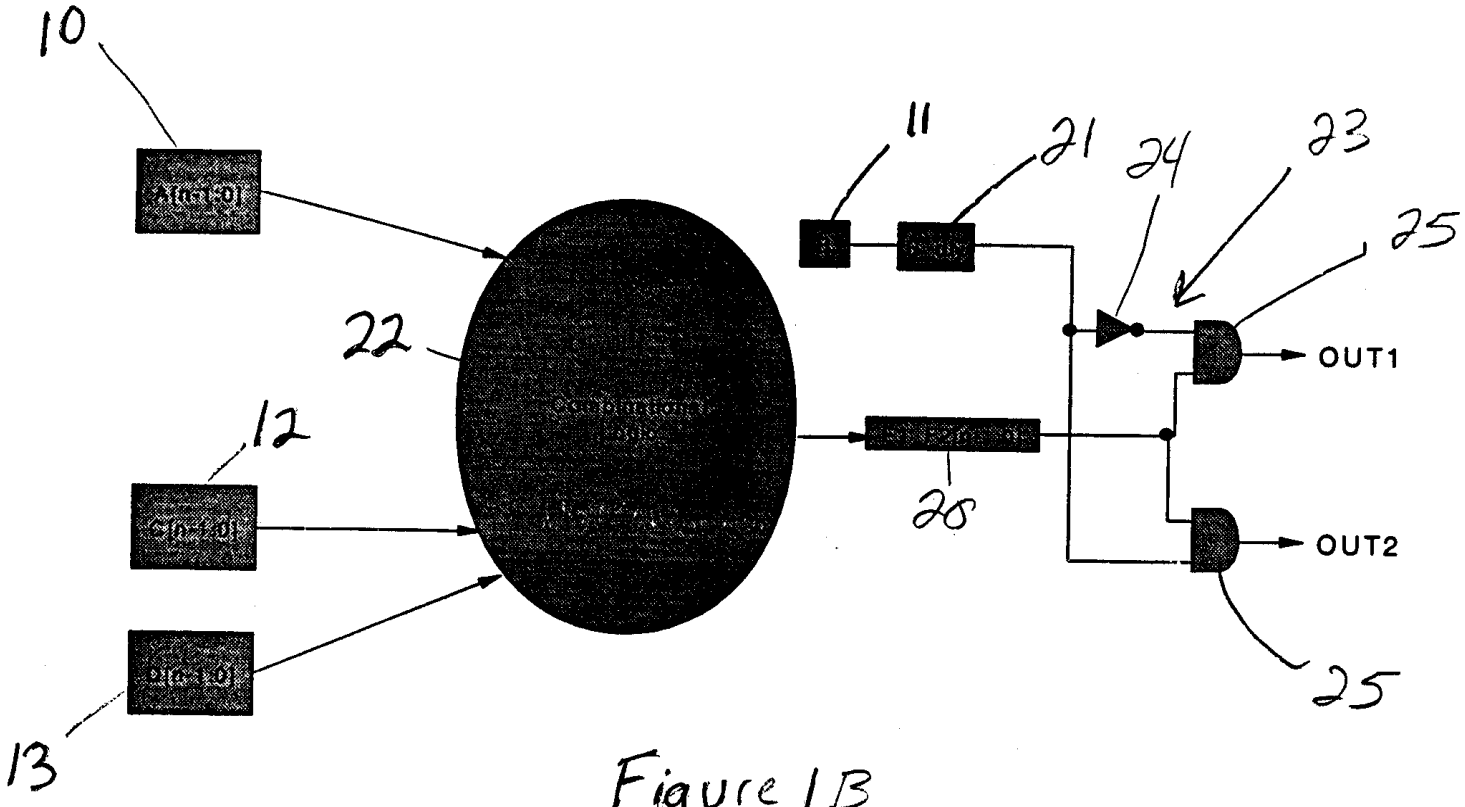

Figure 1B

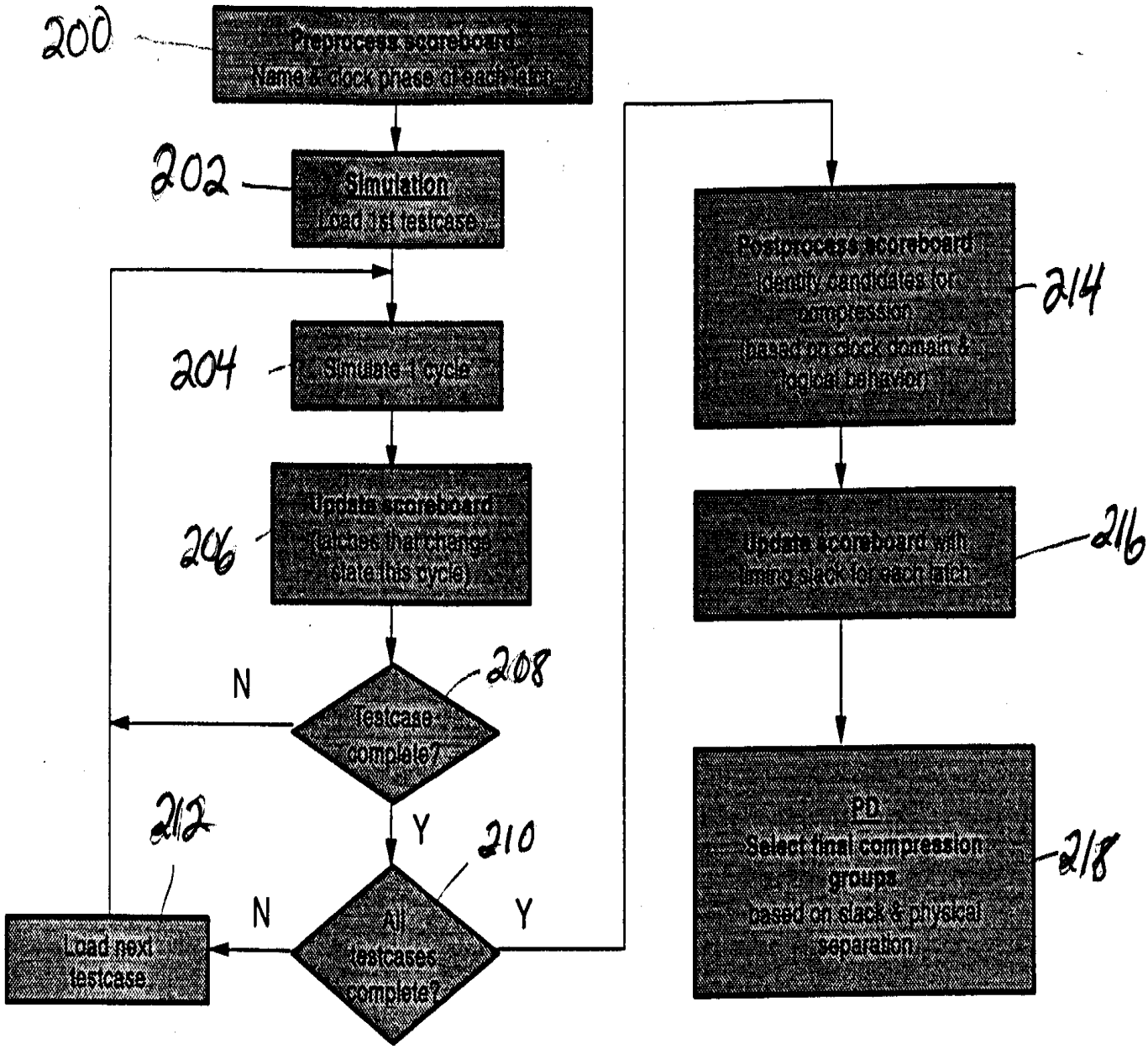
200
Preprocess scoreboard
Name & clock phase of each latch
202
Simulation
Load 1st testcase
204
Simulate 1 cycle
206
Update scoreboard
(latches that changed state this cycle)
208
Testcase complete?
N
Y
210
All testcases complete?
N
Y
212
Load next testcase
214
Postprocess scoreboard
identify candidates for compression
(based on clock domain & logical adjacency)
216
Update scoreboard with timing slack for each latch
218
PD
Select final compression groups
based on slack & physical separation

Figure 2